IN THE CLAIMS

1. (Currently Amended) A method of forming an active device, the method comprising:

performing a first patterning operation having a first pattern on a first plurality of layers comprising etching the first plurality of layers into a first plurality of strips oriented in a first direction, the first patterning operation defining a first feature of the active device; and

performing a second patterning operation having a second pattern ~~different from the first pattern~~ comprising etching at least one strip of the first plurality of strips in a second direction, the second direction being different than the first direction to create a pillar on at least one patterned layer of the first plurality of layers, the second patterning operation defining a second feature of the active device, wherein the first and second patterning operations are performed substantially back-to-back.

~~2.~~ (Currently Amended) The method of Claim 1, wherein the ~~first patterning operation includes:~~

~~etching the~~ first plurality of layers ~~into a first plurality of strips oriented in a first direction~~ includes at least one of a P-type layer and an N-type layer.

~~3.~~ (Currently Amended) The method of Claim 2, wherein a three-dimensional array of diodes is formed. ~~the second patterning operation includes:~~

~~etching at least one strip of the first plurality of strips in a second direction, the second direction being different than the first direction, to create a pillar.~~

4. (Currently Amended) The method of ~~Claim 3~~ Claim 1, wherein at least one strip of the first plurality of strips comprises a first terminal of the active device.

5. (Original) The method of Claim 4, wherein the pillar comprises another portion of the active device.

6. (Original) The method of Claim 4, further including:

depositing a first dielectric after both first and second patterning operations; and

planarizing the first dielectric to expose a surface of the active device.

7. (Original) The method of Claim 6, further including performing a cleaning step after planarizing.

8. (Original) The method of Claim 6, further including:

depositing a second plurality of layers on the surface of the active device and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

9. (Original) The method of Claim 8, wherein said second plurality of strips is not self-aligned in the pillar.

10. (Original) The method of Claim 8, wherein at least one strip of the second plurality of strips comprises a second terminal of the active device.

11. (Original) The method of Claim 1, wherein the first plurality of layers include an antifuse layer fully etched through by the first patterning operation, but not fully etched through by the second patterning operation.

12. (Original) The method of Claim 1, wherein the first plurality of layers includes an antifuse layer fully etched through by both the first and second patterning operations.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) The method of ~~Claim 15~~ Claim 1, wherein the first plurality of strips include first terminals of ~~the~~ an array of diodes.

17. (Currently Amended) The method of ~~Claim 15~~ Claim 1, wherein unetched strips of the first plurality of strips comprise a portion of ~~the~~ an array of diodes and etched strips of the first plurality of strips comprise another portion of the diodes.

18. (Original) The method of Claim 16, further including:

depositing a first dielectric after first and second patterning operations; and

planarizing the first dielectric to expose a surface of the diodes.

19. (Original) The method of Claim 18, further including performing a cleaning step following planarization.

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Currently Amended) The method of ~~Claim 14~~ Claim 16, wherein the first plurality of layers includes an antifuse layer fully etched through by the first and second patterning operations.

24. (Currently Amended) The method of ~~Claim 21~~ Claim 16, wherein the array is a three-dimensional array and a portion of the second plurality of strips is etched in the first direction to form another plane of diodes.

25-33 (Cancelled)

34 (Cancelled)

35. (Currently Amended) A method of forming an active device~~, the method~~ of Claim 1 further comprising:

~~performing a first patterning operation on a first plurality of layers,~~ the first patterning operation defining a first terminal of the active device;

~~performing a second patterning operation on at least one patterned layer of the first plurality of layers,~~ the second patterning operation defining a first feature of the active device~~,~~; ~~wherein the first and second patterning operations are performed substantially back-to-back;~~ and

performing a third patterning operation on a second plurality of layers, wherein the third patterning operation defines a second feature and a second terminal of the active device.

36. (Cancelled)

37. (Cancelled)

38. (Currently Amended) The method of ~~Claim 37~~ Claim 35, further including:

depositing a first dielectric after both first and second patterning operations; and

planarizing the first dielectric to expose a surface of the active device.

39. (Original) The method of Claim 38, wherein performing the third patterning operation is preceded by steps including:

depositing a second plurality of layers on the surface of the active device and the first dielectric; and

etching the second plurality of layers into a second plurality of strips oriented in the second direction.

40. (Original) The method of Claim 39, wherein at least one strip of the second plurality of strips comprises the second feature, and wherein at least one other strip of second plurality of strips comprises the second terminal of the active device.

41. (Currently Amended) The method of ~~Claim 38~~ Claim 6, further including growing antifuse material on the exposed surface of the active device.

42. (Currently Amended) ~~A~~ The method of forming ~~diodes in an array, the method comprising~~

~~performing a first patterning operation on a first plurality of layers,~~ an active device of Claim 1, the first plurality of layers including a first silicon-type layer~~, the first patterning operation forming a first plurality of strips~~; and

~~performing a second patterning operation on at least one layer of the first plurality of strips,~~ the second patterning operation defining one feature of a plurality of diodes from the first silicon-type layer. ~~, wherein the first and second patterning operation are performed substantially back-to-back.~~

43. (Cancelled)

44. (Cancelled)

45. (Original) The method of Claim 42, wherein the first plurality of strips include first terminals of the diodes.

46. (Original) The method of Claim 45, further including:

depositing a first dielectric after first and second patterning operations; and

planarizing the first dielectric to expose a surface of the diodes.

47. (Original) The method of Claim 46, further including performing to HF dip following planarizing.

48. (Cancelled)

49. (Currently Amended) The method of ~~Claim 48~~ Claim 45, wherein the second plurality of strips include second features and second terminals of the diodes.

50. (Original) The method of Claim 46, further including growing antifuse material on the exposed surfaces of the diodes.

51. (Currently Amended) The method of ~~Claim 48~~ Claim 50, wherein the ~~array is~~ diodes form a three-dimensional array and a portion of the second plurality of strips are etched in the first direction to form features of another plane of diodes.

52. (Currently Amended) ~~A~~ The method of ~~isolating pillars on an integrated circuit, the method including~~ forming an active device of Claim 1 wherein the first patterning operation comprises

~~performing~~ a first anisotropic etch ~~on a~~ the first plurality of layers~~, thereby forming patterned structures;~~ and

~~performing~~ the second patterning operation comprises a second anisotropic etch. ~~on the patterned structures, thereby forming the functional pillars, wherein the first and second anisotropic etches are performed substantially back-to-back.~~

53. (Original) The method of Claim 52, wherein the first plurality of layers includes at least one silicon-type layer.

54. (Original) The method of Claim 52, wherein the first plurality of layers includes at least one refractory metal layer.

55. (Original) The method of Claim 52, wherein the first plurality of layers includes an antifuse layer.

56. (Currently Amended) ~~A~~ The method of forming ~~diodes in an array, the method comprising:~~

~~performing a first patterning operation on a first plurality of layers,~~ an active device of Claim 1 wherein the first plurality of layers ~~including~~ includes an N layer and two P+ layers sandwiching an antifuse layer~~, the first patterning operation forming a first plurality of strips~~; and

~~performing a~~ the second patterning operation is performed on at least the N layer of the first plurality of strips. ~~wherein the first and second patterning operations are performed substantially back-to-back.~~

57. (Cancelled)

58. (Cancelled)

59. (Currently Amended) The method of ~~Claim 58~~ Claim 56, wherein the first plurality of strips ~~the first plurality of strips~~ include terminals of ~~the~~ an array of diodes.

60. (Original) The method of Claim 59, wherein unetched strips of the first plurality of strips comprise first terminals of the diodes and etched strips of the first plurality of strips comprise at least a portion of the diodes.

61. (Original) The method of Claim 60, further including:

depositing a first dielectric after first and second patterning operations; and

planarizing the first dielectric to expose a surface of the diodes.

62. (Original) The method of Claim 61, further including performing a cleaning step following planarization.

63. (Cancelled)

64. (Cancelled)

65. (Original)

66. (Original) The method of Claim 56, wherein the first plurality of layers includes the antifuse layer fully etched through by the first and second patterning operations.

67. (Currently Amended) The method of ~~Claim 64~~ Claim 60, wherein the array is a three-dimensional array and a portion of the second plurality of strips are etched in the first direction to form another plane of diodes.

68-70 (Cancelled)